**IN THE TITLE:**

Please amend the Title as follows:

~~PROCESS FOR MANUFACTURING~~ INTEGRATED RESISTIVE ELEMENTS WITH SILICIDATION PROTECTION

**IN THE SPECIFICATION:**

Please amend paragraph [20] as follows:

[20] With reference to FIGURES 8 and 9a, a thin oxide layer 18, having a thickness of a few nanometers ~~nanometres~~, is grown above the active area 15, and subsequently a pair of mutually symmetrical polysilicon delimiters 20 are formed. In particular, a polysilicon layer ~~20', represented in FIGURE 8 by a dashed line,~~ is formed on the wafer 10 and subsequently defined so as to form the delimiters 20. Preferably, the polysilicon layer ~~20'~~ coats the entire wafer 1 and is used also for fabricating other integrated components (not illustrated here) such as, for example, MOS transistors or memory cells either of a volatile type or of a non-volatile type. The delimiters 20 have a height H, extend parallel to one another for respective portions 20a facing each other, at a predetermined distance L apart, and then diverge at their respective ends 20b, following a broken polygonal line. Preferably, the distance L is approximately twice the height H of the delimiters 20. Alternatively (FIGURE 9b), delimiters 50 have ends 50b forming predetermined angles with respective central portions 50a. The oxide layer 18 is then removed outside the delimiters 20.